Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	10/042,080	BERRY ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2133	

All Participants:

(1) *John P. Trimmings*.

(2) *Dustin Mauck*.

Status of Application: _____

(3) _____.

(4) _____.

Date of Interview: *28 July 2005*

Time: *9:00 am*

Type of Interview:

☒ Telephonic
☐ Video Conference
☐ Personal (Copy given to: ☐ Applicant ☐ Applicant's representative)

Exhibit Shown or Demonstrated: ☐ Yes ☒ No
If Yes, provide a brief description:

Part I.

Rejection(s) discussed:

Claims discussed:
10

Prior art documents discussed:

Part II.

SUBSTANCE OF INTERVIEW DESCRIBING THE GENERAL NATURE OF WHAT WAS DISCUSSED:
See Continuation Sheet

Part III.

☒ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview directly resulted in the allowance of the application. The examiner will provide a written summary of the substance of the interview in the Notice of Allowability.

☐ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview did not result in resolution of all issues. A brief summary by the examiner appears in Part II above.

(Examiner/SPE Signature)

(Applicant/Applicant's Representative Signature – if appropriate)

Continuation of Substance of Interview including description of the general nature of what was discussed: Claim 10 was the subject of an agreement by Mr. Mauck with the examiner wherein the claim is amended as follows:

10. (Currently Amended) A method for enhancing test coverage in a level-sensitive scan design (LSSD), the method comprising the steps of:
receiving and temporarily storing a first scan data bit;
transmitting the first scan data bit from a first SRL through a logic unit to a second SRL if there is a logic 0 control signal;
receiving and temporarily storing a second scan data bit;
generating an inverted bit of the first scan data bit if there is a logic 1 control signal;
generating a first output data bit by receiving the first and second scan data bits;
transmitting the first output data bit to a last SRL within the SRL chain;
generating a second output data bit by receiving the inverted bit and the second scan data bit;
transmitting the second output data bit to the last SRL within the SRL chain; and
enhancing test coverage of combinational logic by obtaining a result from both the first and second output data bits.

John P Trimmings
Examiner